REMARKS/ARGUMENTS

Claims 1-28 are pending in this application. Claims 1, 10 and 20 are amended.

Claim rejections -35 U.S.C. § 102

The Patent Office rejected claims 1-5, 10-14 and 20-24 under 35 U.S.C. § 102 for being anticipated by Irrinki et al. ("Irrinki", U.S. Patent No. 6,067,262). Applicants respectfully traverse.

The present invention is directed to a method and system which allows a chip level scan test to be performed without altering a normal custom testing flow for integrated circuits. Generally, a custom testing flow is used for integrated circuits having a BISR circuit. Typical BISR stores its repair information in soft latches during a BISR run and the repair information is scanned out whenever the user needs the repair information. However, the repair information will not be available when a chip level scan test is performed in the middle of the custom test flow. The method and system of the present invention preserves the repair information of BISR regardless of the order of the testing flow (i.e. the scan test may be done at any point of the testing flow). Thus, the method and system of the present invention allows a user to have an optimal test flow that may employ the chip level scan test and BISR.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Applicants respectfully submit claims 1, 10 and 20, include elements that have not

been disclosed, taught or suggested by Irrinki. For example, Claims 1, 10 and 20 recites "said scan test is any part of said custom test flow employing a BISR circuit" or "a scan test as a part of a custom test flow."

Accordingly, Applicants respectfully submit that *prima facie* cases of anticipation of claims 1, 10 and 20 have not been established. Removal of the pending rejections to Claim 1, 10 and 20 under 35 U.S.C. §102 is respectfully requested. Claims 2-5 depend on Claim 1. Claims 11-14 depend on Claim 10. Claims 21-24 depend on Claim 20. Claims 2-5, 11-14, and 21-24 are therefore believed to be allowable due to their dependency on allowable base Claims.

Claim Rejections – 35 U.S.C. § 103

The Patent Office rejected claims 6, 15, and 25 under 35 U.S.C. § 103(a) as being unpatentable over Irrinki. Claims 7-9, 17-19 and 26-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Irrinki in view of Fosco et al. ("Fosco", U.S. Patent No. 6,212,656). Claim 16 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Irrinki in view of Hatada ("Hatada", U.S. Patent No. 6,408,414). Applicants respectfully traverse these rejections.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970).

Further, "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988).

Claims 6 and 14 stand rejected under 35 U.S.C. §103(a). As indicated in the foregoing *Claim Rejections – 35 USC § 102* section, Claims 1 and 10 are believed allowable. Therefore, Claims 1 and 10 are nonobvious under 35 U.S.C. §103. Claim 6 depends on Claim 1 and Claim 14 depends on Claim 10. Therefore Claims 6 and 14 are nonobvious under 35 U.S.C. §103 due to their dependency.

Regarding the rejections in Claims 7-9, 16-19 and 26-28, as indicated in the foregoing *Claim Rejections – 35 USC § 102* section, Claims 1, 10 and 20 are believed allowable. Additionally, the ancillary reference, Fosco, does not teach the elements of Claims 1, 10 and 20. Fosco merely teaches a method and apparatus for an automated technique of creating multiple scan chains, each of any desired length, within the same test circuitry design. Thus, Fosco, either alone or in combination with Irrinki, fails to teach or suggest all the elements recited in Claims 1, 10 and 20. Moreover Hatada does not disclose, teach, or suggest the elements of Claims 1, 10 and 20 since Hatada merely teaches a semiconductor device provided with a compact boundary-Scan test circuit.

Therefore, Claims 1, 10 and 20 are nonobvious under 35 U.S.C. §103. Claims 7-9 depend on Claim 1 and Claims 17-19 depend on Claim 10. Claims 26-28 depend on Claim 20. Accordingly, Claims 7-9, 17-19 and 26-28 are nonobvious under 35 U.S.C. §103 due to their dependency. Withdrawal of the rejections of all claims under 35 U.S.C. § 103 is therefore respectfully requested.

CONCLUSION

In light of the foregoing amendments and remarks, Applicants respectfully request a timely Notice of Allowance.

Respectfully submitted,

LSI Logic Corporation,

Dated: June 14, 2004

By: _____
Sunah K. Lee
Reg. No. 53,198

Sunah K. Lee
SUITER – WEST PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile